Amendments to the Drawings:

Applicants are amending Fig. 3 herein, to more particularly show the selector parameter to the MUX of that figure. A corrected drawing sheet is included herewith, as is an annotated sheet showing the changes made.

Attachment: One (1) Replacement Sheet
One (1) Annotated Sheet Showing Changes

Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claim 8 is presently pending in the application. Former claims 3 and 4 have been canceled from the present application. Claims 1 - 2 and 5 - 7 were previously canceled. New claim 8 has been added to the application.

In item 3 of the above-identified Office Action, the drawings were objected to because Fig. 3 was missing the selector parameter to the MUX that selects between the two inputs. A corrected drawing sheet addressing the concern raised in item 3 of the Office Action, as well as an annotated drawing sheet showing the changes made, are submitted herewith.

In item 6 of the Office Action, Applicants' former claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,854,913 to Goetz et al ("**GOETZ**"), in view of U. S. Patent No. 5,088,030 to Yoshida ("**YOSHIDA**") [sic], Mano and Kime, "Logic and Computer Design Fundamentals" ("**MANO**"), "The PowerPC Architecture", 1994 ("**POWERPC**") and K. Short, "Embedded Microprocessor Systems Design"; 1998 ("**SYSTEMS DESIGN**").

Applicants respectfully traverse the above rejections. First, Applicants have canceled claims 3 and 4 from the instant application, and thus believe that the above-rejections are moot as to those claims.

Additionally, Applicants' believe that the presently presented claim 8 is patentable over the combination of **GOETZ**, **YOSHIDA MANO**, **POWERPC** and **SYSTEMS DESIGN**.

More particularly, Applicants' new claim 8 recites, among other limitations:

> a multiplexer having a first input, a second input for receiving a 0 value, and a third input **receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;**
>
> . . .
>
> **an adding unit connected between said program counter and said computation unit**, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, **a third input receiving the parameter** and an output connected to said computation unit;
>
> **a subtracting unit connected between said program counter and said computation unit for the relative addresses**, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, **a third input receiving the parameter** and an output connected to said computation unit; [emphasis added by Applicants]

As such, Applicants' new claim 8 requires, among other things, **both an adding unit and a subtracting unit, each of which**

receives a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place (i.e., the parameter designating the respective assembler code also being used to select whether the adding unit or the subtracting unit is used). That the parameter is used to designate the assembler code, as recited in Applicants' new claim 8, is supported by the specification of the instant application, for example, on page 3, lines 21 - 26, which states:

> According to the invention, the object is achieved by a microprocessor for processing various assembler codes, in that **the parameter that designates the respective assembler code is provided** and, **dependent on the parameter, a different relative addressing takes place.**

Additionally, Applicants' specification supports the use of **both an adding unit and a subtracting unit in the same device.**

For example, page 11 of the instant application, lines 13 - 16, state:

> **According to a fourth embodiment of the invention**, the value of the instruction length may also **be added** to an offset value which is used for the computation of the relative addresses, **or may be subtracted** from the offset value. [emphasis added by Applicants]

See also, page 5 of the instant application, line 18 - page 6, line 4, states:

> Similarly, it is preferably possible according to the invention, **dependent on the various operating states or assembler codes, to add or subtract the instruction length to or from the program counter reading for the relative address computation**, or to leave the program counter reading unchanged.
>
> **Similarly, it is possible according to the invention, dependent on the various operating states or assembler codes, to add, or subtract, an instruction length to or from the offset value**, which is usually used for the computation of relative addresses, or to leave the offset value unchanged in each case. [emphasis added by Applicants]

Further, page 12 of the instant application, lines 13 - 25, describes **the operation of the fourth embodiment of the instant invention having a single device incorporating both adding and subtracting units**, stating:

> According to the invention, for example, when using the address of the current instruction line in the instruction counter of the microprocessor, **the instruction length can then optionally be added to the offset value** if using an assembler that specifies that the instruction counter must point to the next assembler instruction.
>
> Similarly, **when managing the address of the next assembler instruction** in the instruction counter of the processor, **the instruction length can be subtracted from the offset value** if an assembler for which the instruction counter must always point to the current assembler instruction is to be processed. [emphasis added by Applicants]

As such, Applicants' specification describes at least one embodiment of the invention **wherein a first instruction can be addressed by adding the instruction length to an offset value, while the very next instruction can be differently relatively**

addressed by subtracting the instruction length from the offset value.

In view of the foregoing, it is believed that Applicants' specification supports the new claim 8, which recites, among other limitations, both an adding unit and a subtracting unit.

However, the references cited in the Office Action fail to teach or suggest **including**, among other limitations of Applicants' claim, **both an adding unit and a subtracting unit, each of which receives a parameter** designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place.

More particularly, page 8 of the Office Action states, in part:

> Goetz, Yoshida, Mano, May and Short fail to teach the only limitation different from claim 3, **which is "a subtracting unit"** instead of an "**adding unit**". [emphasis added by Applicants]

The Office Action further goes on to state, in part:

> However, Examiner takes Official Notice that numbers, including offsets, are very frequently represented in two's complement form, which allows simplified binary arithmetic operation.
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the offsets represented in two's complement form since

> Examiner takes Official Notice two's complement form allows simplified binary arithmetic operations.
>
> It is inherent that a binary adder is also a subtraction unit if the binary inputs are in two's complement form, because there is no difference in hardware between adding two's complement numbers and subtracting two's complement numbers. A two's complement adder is inherently a subtraction unit as well.

Applicants' respectfully traverse the above-argument made on page 8 of the Office Action, but believe that the above-argument is mooted by the present language of the claim.

More particularly, Applicants' new claim 8, recites two separate units, one being an adding unit, the other being a subtracting unit, each of which receives a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place (i.e., the parameter designating the respective assembler code choosing whether the adding unit or the subtracting unit is used).

Even taking into consideration, arguendo, the arguments made on page 8 of the Office Action, the cited references would not teach or suggest, alone or in combination, Applicants' claimed invention including **two** units, one of which being an adding unit, the other being a subtracting unit, each receiving the parameter designating the respective assembler code. In fact,

the logic on page 8 of the Office Action would, if taken, arguendo, as correct would teach a person of skill in the art **away** from Applicants' claimed invention, by causing the person of skill in this art to conclude that there was no need for two different units, wherein, per the allegation in the Office Action that "a binary adder is also a subtraction unit if the binary inputs are in two's complement form." Thus, a person of ordinary skill in the art, reading **GOETZ**, **YOSHIDA MANO**, **POWERPC** and **SYSTEMS DESIGN** would not be taught, suggested or motivated to provide **both an adding unit and a subtracting unit, each of which receives a parameter** designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place, as required by Applicants' claim 8.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. The presently cited references do not provide the necessary teaching, suggestion or motivation that would lead a person of ordinary skill in the art to Applicants' presently claimed invention.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claim 8. Claim 8 is, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claim 8 is solicited.

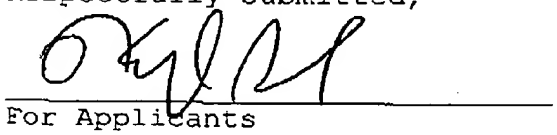
In the event the Examiner should still find the claim to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

The instant amendment is being filed simultaneously with a Request for Continuing Examination and its associated fee. Additionally, please consider the present as a petition for a three (3) month extension of time, and please provide a three (3) month extension of time, to and including, February 28, 2007 to respond to the present Office Action.

The extension fee for response within a period of three (3) months pursuant to Section 1.136(a) in the amount of $1,020.00 in accordance with Section 1.17 is enclosed herewith.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



For Applicants

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February 27, 2007

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FIG 1

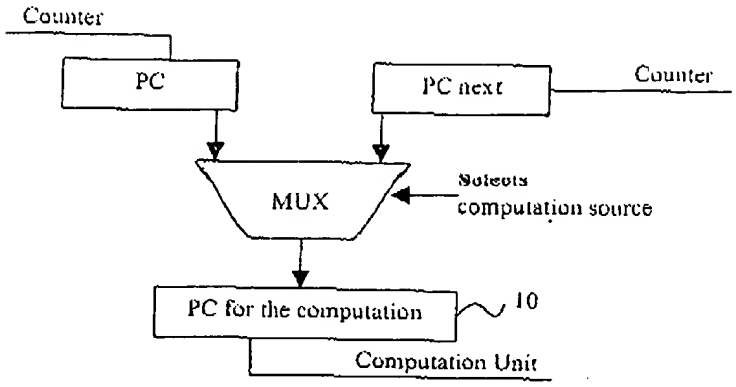

FIG 2

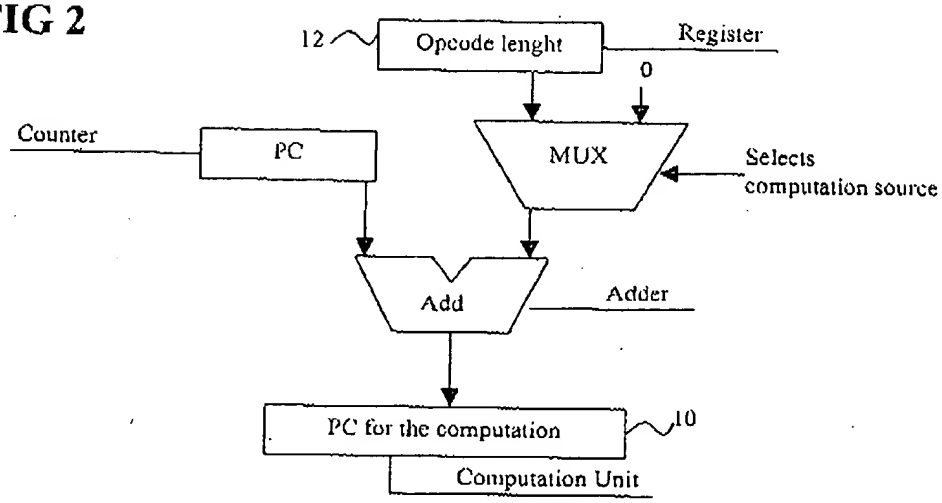

FIG 3